

6.002 Demo# 12

Gate Ringing

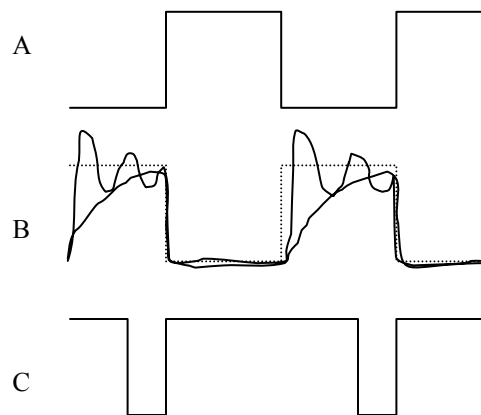
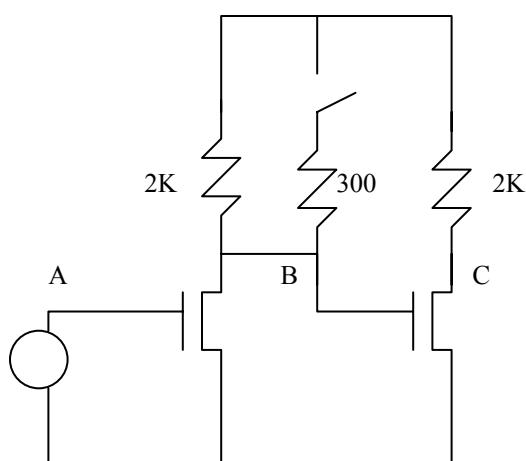
Lecture 15

Agarwal Fall 2000

Purpose: This demo examines second order responses using two cascaded inverters. By lowering R_L in the first inverter (in an attempt to speed up the RC delay), the middle voltage (between the two inverters) is shown to ring. This is caused by inductance in the loop between ground and the middle voltage.

Steps:

1. Show the input, middle and output voltages for the circuit with R_L set at the high value (2kOhm). Note the RC behavior of the middle voltage, and the resulting delay at the output.
2. Switch the 300 Ohm resistor into the circuit. Observe the ringing behavior in the middle voltage.



Description: Gate Ringing

To show the ringing taking place, set the switch on the board to on position and observe CH1 , CH2 and CH3.

Note: for schematic diagram and pins output, see next page Fg 1 and Fg2 for more detail.

Oscilloscope Setup

CH	V/DIV	OFFSET	MODE	FUNC	MATH	VERTICAL	HORIZONTAL
1 on	5	-9.31	DC	off			
2 on	5	170	DC	off			
3 on	5	9.70	DC	off			
4 off				off			
Horizontal: 1 us/Div		Acquisition:		Trigger: CH1			

Waveform Generator Setup

Power Supply Setup

UNIT	WAVE	AMP	OFFSET	FREQ	+6	+25	-25	OUTPUT
FG1	Square	5	2.5	5 KHZ	0	5		on

Note: FG1 should be set @ Hi Z

Gate Ringing

